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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,134	10/09/2003	David Arnold Luick	ROC920020127US1	1346

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,134	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-15,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 29, 2006 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the elements in claim 21, such as "for each of the plurality of secondary latches, performing the steps of: ..." and the elements in claim 22 "wherein the context switch performed in step (D) occurs in a single clock cycle" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 9-15, 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Referring to claim 9, the limitation "a register file bit comprising: a primary latch ... a plurality of secondary latches ..., a feedback path ... a context switch mechanism ..." is not clear. It is not understood how a single bit can comprise hardware, such as the claimed latches, the feedback path and the context switch mechanism. For the purposes of examination "a register file bit" is interpreted as "a register file". Appropriate correction is required.

8. Dependent claims 10-15 are rejected for incorporating the defects of independent claim 9.

9. Claim 10 is unclear. How can a signal be coupled to hardware as in line 2: "a swap signal coupled to the primary latch". Hardware can only be coupled to hardware. For the purposes of examination, the limitation will essentially be interpreted as "a medium carrying/storing a swap signal coupled to the primary latch". Appropriate correction is required.

10. Claim 21, lines 5 and 6 and contain the following limitation "storing a value in the primary latch that corresponds to a selected thread" and line 8 contains the following limitation "storing a value in the primary latch that corresponds to an active thread". Is the value in lines 5 and 6 the same as the value in line 8? Is an active thread the same as a selected thread? For the purpose of examination the value in lines 5 and 6 is interpreted as the value in line 8 since any active thread has also been selected.

11. In claim 21, line 12, does "the value in the primary latch" correspond to the value in line 5 or line 8. For purposes of examination all three claimed values in lines 5, 8 and 12 are treated as the same value. Appropriate correction is required.

12. In claim 21, line 4, the limitation "for each of the plurality of secondary latches, performing the steps of:..." does not make clear whether the steps performed for each of the plurality of secondary latches include (A1), (A2), (B), (C) and (D), or just (A1) and (A2). Furthermore, examiner attempted to clarify the claim and couldn't find any support for performing any of the selected steps for each of the plurality of secondary latches in the specification. Examiner only located performing the steps of (A1) and (A2) for one of

the plurality of secondary latches (see specification, page 7, lines 11-26). For the purposes of examination, the limitation is essentially interpreted as "for one of the plurality of secondary latches, performing the steps of: (A1) and (A2)". Appropriate correction is required.

13. Dependent claim 22 is rejected for incorporating the defects of independent claim 21.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 9-15 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Henry et al., US Patent 6,145,075 (Herein referred to as "Henry").

16. Referring to claim 9, Henry has taught an integrated circuit comprising:

a. a register file bit (This is interpreted as a register file, see the 112 rejection above., Figure 5, element 506) comprising:

b. a primary latch (Figures 5 and 6, R1 in register file 306) having a data input (Figures 5 and 6, elements 550 and 552) and a data output (Figures 5 and 6, outputs from element 506 to elements 545 and 547);

c. a plurality of secondary latches (Figures 5 and 6, register file 306 (except for R1 which is the primary latch)) each having a data input (Figures 5 and 6,

elements 550 and 552) and a data output (Figures 5 and 6, The outputs from element 506 to elements 545 and 547.);

d. a feedback path from the data outputs of the plurality of secondary latches to the data input of the first primary latch (Figures 5 and 6, At least elements 545, 547, 508, 510, 512, 513, 550, 552 and 560 comprise the feedback path.), the feedback path including a data selection mechanism for selecting one data output only from among each of the data outputs from the plurality of secondary latches to feed back to the data input of the first primary latch (column 6, line 40-column 7, line 47, Upon an exchange instruction, the data to be stored in R1 is selected only from among the registers in the register file, element 506.); and

e. a context switch mechanism (abstract, Figure 5 is a mechanism that switches values in a microprocessor environment, or context. Figure 5 is the context switch mechanism.) that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches (column 6, line 40-column 7, line 47, Output from R1 is written to R2), and that causes the data on the data output of the selected one secondary latch to be written to the primary latch (column 6, line 40-column 7, line 47, Output from R2 is written to R1).

17. Referring to claim 10, Henry has taught the integrated circuit of claim 9, as described above and wherein the context switch mechanism comprises a swap signal coupled to the primary latch (Figure 5, at least elements 541, 543, 540, 550 and 552

each comprise the claimed swap signal as they are all signals in a mechanism that performs a swap.).

18. Referring to claim 11, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches (Figure 5, At least elements 512, 513, 545, 547, 508, 510, 560, 550 and 552 each comprise the claimed delay element in the feedback path.).

19. Referring to claim 12, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 5, At least elements 512, 513, 545, 547, 508, 510, 560, 550 and 552 each comprise the claimed delay element).

20. Referring to claim 13, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch (column 6, line 40-column 7, line 47, column 8, lines 48-50, A clocked system latches data based on a clock signal. This is a clocked system, so the register data is latched through the system (input and output) based on the clock.) and at least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch (column 6, line 40-column 7, line 47, column 8, lines 48-50, A clocked system latches data based on a clock signal. This is a clocked system, so the register data is latched through the system (input and output) based on the clock.).

21. Referring to claim 14, Henry has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of write ports on the data input of the primary latch (Figure 5, elements 550 and 552 and ports carrying elements 541 and 543 comprise the claimed write ports.).

22. Referring to claim 15, Henry has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of read ports on the data output of the primary latch (Figure 5, The ports carrying elements 545 and 547 comprise the claimed read ports.).

23. Referring to claim 21, Henry has taught a method for performing a fast context switch in a register file (Figure 5, element 506) that includes a primary latch (Figures 5 and 6, R1 in register file 306) and a plurality of secondary latches (Figures 5 and 6, register file 306 (except for R1 which is the primary latch)) having data outputs (Figures 5 and 6, The outputs from element 506 to elements 545 and 547.), the method comprising the steps of:

(A) for each of the plurality of secondary latches, performing the steps of (This is interpreted as "for one of the plurality of secondary latches, performing the steps of: (A1) and (A2)". See the 112 rejection above.):

(AI) storing a value in the primary latch that corresponds to a selected thread (column 7, lines 35-46, A value is stored in R1 in response to a selected process, or thread, containing an exchange instruction.);

(A2) moving the value in the primary latch to a secondary latch (column 2, lines 6-9, column 7, lines 35-47, R1 is moved to R2);

(B) storing a value in the primary latch that corresponds to an active thread (column 7, lines 35-46, A value is stored in R1 in response to an active process, or thread, containing an exchange instruction.);

(C) selecting one data output only from among each of the data outputs of the secondary latches for performing a context switch with the primary latch (abstract, Figure 5 is a mechanism that switches values in a microprocessor environment, or context., column 6, line 40-column 7, line 47, Upon an exchange instruction, the data to be stored in R1 is selected only from among the registers in the register file, element 506. R1 is selected to be switched with R2.); and

(D) performing a context switch (abstract, Figure 5 performs a switch of values in a microprocessor environment, or context.) between the primary latch and the selected one secondary latch that causes the value in the primary latch to be stored in the selected one secondary latch (column 2, lines 6-9, column 7, lines 35-47, R1 is stored in R2.), and that causes the value in the selected one secondary latch to be stored in the primary latch (column 2, lines 6-9, column 7, lines 35-47, R2 is stored in R1.).

24. Referring to claim 22, Henry has taught the method of claim 21, as described above, and wherein the context switch performed in step (D) occurs in a single clock cycle (column 2, lines 6-9, column 7, lines 35-47).

Response to Arguments

25. Applicant's arguments with respect to claims 9-15, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Daniel et al., US Patent 5,987,258, has taught swapping register contents when an interrupt occurs.

b. Landau, Jr., et al., US Patent 4,092,937, has taught swapping a PSW register with the A or B register upon an interrupt.

c. Elkateeb, "The impact of Using the RISC Architecture in the Network Nodes", IEEE, has taught independent sets of registers holding a context of a task and moving the register values on a context switch.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

tlm

TONIA L. MEONSKE
DECEMBER 8, 2006
Tonia L. Meonske